REMARKS

This responds to the Office Action mailed on August 15, 2006, and the references cited therewith.

Claims 1, 2, 4, 6, 8, 9, and 11 are amended; no claims are canceled; and claims 18-22 are added; as a result, claims 1-22 remain pending in this application.

§103 Rejection of the Claims

According to *M.P.E.P.* § 2141, which cites *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986), the following tenets of patent law must be adhered to when applying 35 U.S.C. § 103. First, the claimed invention must be considered as a whole. Second, the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination. Third, the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention. Fourth, obviousness is determined using a reasonable expectation of success standard. Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. *M.P.E.P.* § 2141 (citing *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966)).

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d, 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Claims 1-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Schimmel (US 6,105,113; hereinafter "Schimmel") and in view of Scott et al. (US 6,925,547; hereinafter "Scott").

Applicant respectfully submits that neither Schimmel nor Scott, alone or in combination, teach or suggest a method and system for remote virtual address translation as taught by Applicant and claimed in claims 1-17.

Schimmel describes a system and method for maintaining Translation Took-aside Buffer (TLB) consistency. Specifically, Schimmel describes automatically a method and system for keeping a TLB in a local node consistent with current changes in page table entries by its operating system without interrupting its CPU or operating system.

Scott describes a method for performing remote address translation in a multiprocessor system (Abstract, lines 1-2). Specifically, Scott describes an address translation method where a virtual address for a remote node is sent to the remote node and translated into a physical address at the remote node using a translation look-aside buffer (TLB) (*id.* lines 2-19).

Neither Schimmel nor Scott, however, alone or in combination, teach or suggest following elements as taught by Applicant and claimed in amended claims 1, 4, 6, 9 and 11: (1) exporting the local virtual address space for each node to a Remote Translation Table (RTT) associated with that node to build an application virtual address space; and (2) translating a remote node address reference differently depending on whether remote translation is enabled. The Examiner, therefore, has failed to establish a prima facie case of obviousness as required by *In re Fine* and the MPEP as noted above.

In the Office Action, first of all, the Examiner asserts that Schimmel teaches or suggests the exporting process as described and claimed by Applicant (Office Action, p. 6, lines 17-18). As support of this, the Examiner points to col. 1, lines 24-31 of Schimmel, which states:

> In a virtual memory scheme, each process that is allocated a block of physical memory is also provided with a set of translations for translating virtual addresses to assigned physical addresses of the allocated block. Each set of translations can be stored in, for example, a page table. A page table can be associated with a specific user or shared by multiple users. Alternatively, reverse page table techniques can be employed.

Applicant respectfully disagrees with the Examiner's interpretation of Schimmel. Although the cited portion explains general use, dedicated or shared, of a page table for memory translation, it does not teach or suggest that the page table in a main memory contains virtual to physical address translation for remote nodes other than its own local node. In contrast, as noted at p. 3, lines 12-15 and Fig. 9, Applicant explicitly teaches, and claims in claims 1, 4, 6, 9 and 11

that each node exports its local address space to each of a plurality of remote nodes associated with the local node through distribution of an application. Applicant has amended claims 1, 4, 6, 9 and 11 to more clearly emphasize this difference.

In addition, the Examiner asserts that Schimmel teaches or suggests translating a virtual memory reference to a physical address in a remote node using the RTT in a local node (Office Action, p. 8, lines 3-8). As support of this, the Examiner points to col. 4, lines 8-13, col. 7, lines 50-67 and col. 8, lines 1-67 of Schimmel, part of which states:

> (col. 4, lines 8-13) In operation, when a CPU requires a physical memory address that is associated with a virtual memory address, the CPU first searches the virtual address tag of the TLB table, If a valid translation is not found in the TLB table, the translation is retrieved from a cache or from main memory and a copy of the translation is placed in the TLB table.
>
> (col. 7, line 49 through col. 8, line 67) Referring to FIG. 5, a virtual memory address-to-physical main memory address translation scheme 510 is illustrated…Each user or application that is allocated a portion of physical memory can be provided with a separate page table 610. In some cases, page tables can be shared….Thus, a reference F4 will result in a page table miss or page fault and F4 will have to be retrieved from 514….

Applicant respectfully disagrees with the Examiner's interpretation of Schimmel. First of all, as discussed above, none of the cited portions teach or suggest that the page tables of Schimmel contain virtual to physical address translation for other remote nodes. Therefore, the page tables on the local main memory are not used to translate a virtual memory reference for a remote node into a physical address in the remote node. In contrast, Applicant teaches at p. 18, lines 15-20, and claims in claims 1, 4, 6, 9 and 11 that the RTT on the local node is used to translate a virtual address reference from the local node to a remote node, if remote translation mode is enabled. Furthermore, Applicant also teaches, for example, at p. 6, lines 19-21 and p. 15, lines, 12-29, and claims in claims 1, 4, 6, 9 and 11 that Applicant's invention translates a virtual address reference for a remote node differently depending on remote translation mode. Under Applicant's claimed invention, if remote translation is not enabled, the virtual memory address for the remote node is sent to the remote node and translated to a physical address in the remote node using the RTT on the remote node instead of using the RTT on the requesting local node. *Id.* Claims 1, 4, 6, 9 and 11 have been amended to emphasize these differences. Applicant is unable to find such a teaching or suggestion in any of the cited references.

The amended claims are fully supported from the Specification and Figures. Applicant, first of all, teaches that a TLB is used for references to a local node by local processors and that a RTT at the local node is used for memory references from remote nodes to the local node (e.g., fig. 4; page 6, lines 19-21). Also, Applicant teaches that the Vnode (i.e., virtual node) field from a physical address format is used to determine an appropriate node number (e.g., figs. 2-5; page 10, lines 17-18; page 15, lines 14-16). Applicant further teaches that an application virtual address space is built by exporting local virtual address spaces from RTTs to all nodes sharing a job or an application when remote translation is enabled (e.g., page 15, lines 12-29). Finally, Applicant teaches that all valid local translations from several nodes sharing the distributed application are loaded in a RTT in each local node when remote translation is enabled (i.e., once the application virtual address space has completed) (e.g., page 16, lines 6-11).

For the reasons discusses above, neither Schimmel nor Scott, alone or in combination, teach or suggest a method and system for translating remote address references as taught by Applicant and claimed in amended claims 1, 4, 6, 9 and 11. Reconsideration is respectfully requested.

With regard to claims 3, 5, 7 and 10. Claims 3, 5, 7 and 10 are patentable as being dependent on a patentable base claim. In addition, neither Schimmel nor Scott, alone or in combination, teach or suggest synchronizing nodes for completion of exporting RTTs among associated nodes as taught by Applicant and claimed in claims 3, 5, 7 and 10.

In the Office Action, the Examiner states that "in order for the remote translation mechanism disclosed by Schimmel to work and function properly, it is inherent that the RTT at all the nodes be initialized and synchronized first before any reference to a memory location resides at a remote node can be served" (p. 10, lines 5).

Applicant respectfully disagrees. First of all, as discussed above, it is not clear from a reading of Schimmel whether the page tables in each node under Schimmel's approach contain virtual to physical address translation for other remote nodes. Schimmel does not teach or suggest exporting all local translations in each node to each of the associated nodes to build an application virtual address space containing all translation information for all of the associated nodes. Unlike the Examiner's assertion, therefore, it would not necessarily be obvious to one of

ordinary skill in the art at the time of invention to selectively synchronize RTTs of nodes that share an application as taught by Applicant and claimed in claims 3, 5, 7 and 10. Reconsideration is respectfully requested.

With regard to claims 12-17, claims 12-17 are patentable as being dependent on a patentable base claim.

With regard to new claims 18-22, claims 18-22 are supported by the Specification, for example, at page 17, line 23 through page 18, line 2. Claims 18-22 are patentable as being dependent on a patentable base claim. In addition, neither Schimmel nor Scott, alone or in combination, teach or suggest handling request to change the application virtual address space configuration on a node-local basis as taught by Applicant and claimed in claims 18-22.

Double Patenting Rejection

According to *M.P.E.P.* § 804, which cites *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993), a rejection based on nonstatutory double patenting is based on a judicially created doctrine grounded in public policy so as to prevent the unjustified or improper timewise extension of the right to exclude granted by a patent. In determining whether a nonstatutory basis exists for a double patenting rejection, the factual inquires set forth for determining obviousness under 35 U.S.C. 103 in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966) must be shown: (A) the scope and content of a patent claim relative to a claim in the application at issue; (B) the differences between the scope and content of the patent claim as determined in (A) and the claim in the application at issue; (C) the level of ordinary skill in the pertinent art; and (D) evaluation of any objective indicia of nonobviouness. In addition, any obviousness-type double patenting rejection should make clear: (A) the differences between the inventions defined by the conflicting claims – a claim in the patent compared to a claim in the application; and (B) the reasons why a person of ordinary sill in the art would conclude that the invention defined in the claim at issue would have been an obvious variation of the invention defined in a claim in the patent.

If the application at issue is the later filed application or both are filed on the same day, only a one-way determination of obviousness is needed in resolving the issue of double patenting, i.e., whether the invention defined in a claim in the application would have been an obvious variation of the invention defined in a claim in the patent. See, e.g., *In re Berg*, 140 F.3d 1438, 46 USPQ2d 1226 (Fed. Cir. 1998). Similarly, even if the application at issue is the earlier filed application, only a one-way determination of obviousness is needed to support a double patenting rejection in the absence of a finding: (A) of administrative delay on the part of the Office causing delay in prosecution of the earlier filed application; and (B) that applicant could not have filed the conflicting claims in a single (i.e., the earlier filed) application. See M.P.E.P § 804, ¶ II.B.1.(b).

Claims 1-2, 4, 6, 8-9 and 11 were rejected under judicially created doctrine of anticipation-type double patenting as being anticipated by claims 1-35 of U.S. Patent No. 6,922,766 (hereinafter '766). As noted above, determination of one-way obviousness applies here. When applying one-way obviousness test, the Examiner must establish a *prima facie* case of obviousness under 35 U.S.C. § 103 as in the obviousness discussion above.

Applicant respectfully traverses this rejection and asserts that the present claims are patentably distinct from the claims of '766. Each of the independent claims in '766 includes transmitting a remote node virtual memory address from a local node to the remote node which then translates the remote virtual addresses to a physical address in the remote node using the RTT on the remote node. Unlike the claims in '766, for example, Applicant's claimed invention translates a memory reference to a physical address for a remote node differently depending on whether remote translation is enabled. Under Applicant's amended claims, a local node translates a virtual memory address for a remote node on the local node using RTT on the local node if remote translation is enabled. To accomplish this, Applicant teaches that local memory space for each node is exported to all remote nodes sharing an application with the local node. Claims in '766 do not contain such limitations in its claims.

The Examiner, therefore, has failed to establish a prima facie case of obviousness and thereby failed to show satisfying one-way obviousness test as required by *Graham* and *M.P.E.P.* as noted above. In conclusion, Applicant's claimed invention is not anticipated by and patentably

distinct from claims of '766. Claims 1, 4, 6, 9 and 11 have been amended to emphasize these differences. Reconsideration is respectfully requested.

Claims 1-2, 4, 6, 8-9, and 11 were rejected under the judicially created doctrine of "anticipation-type double patenting" as being unpatentable over claims 1, 2, 4, 6, 8-9, and 11 of U.S. App. Serial No. 10/643,588 (hereinafter '588). As noted above, determination of one-way obviousness applies here. When applying one-way obviousness test, the Examiner must establish a *prima facie* case of obviousness under 35 U.S.C. § 103 as in the obviousness discussion above.

Applicant respectfully traverses this rejection and asserts that the present claims are patentably distinct from the claims of '588. Each of the independent claims in '588 includes transmitting a remote node virtual memory address from a local node to the remote node which then translates the remote virtual address to a physical address in the remote node using ERTT Segment on the remote node. Unlike the claims in '588, for example, Applicant's claimed invention translates a memory reference to a physical address for a remote node differently depending on whether remote translation is enabled. Under Applicant's amended claims, a local node translates a virtual memory address for a remote node on the local node using RTT on the local node if remote translation is enabled. To accomplish this, Applicant claims that local memory space for each node is exported to each remote node associated with the local node through an application. Claims in '588 do not contain such limitations in its claims.

The Examiner, therefore, has failed to establish a prima facie case of obviousness and thereby failed to show satisfying one-way obviousness test as required by *Graham* and *M.P.E.P.* as noted above. In conclusion, Applicant's claimed invention is not anticipated by and patentably distinct from claims of '588. Claims 1, 4, 6, 9 and 11 have been amended to emphasize these differences. Reconsideration is respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 14 day of December 2006.

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